REMARKS

In the Office Action dated March 17, 2004, claims 1-28 were presented for examination. Claims 27 and 28 were allowed. Claims 3-7, 12-15, 17, 24, and 26 were objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form to include all of the limitations of the base claim and any intervening claims. Claims 1, 2, 10, 11, 16, 21, 23, and 25 were rejected under 35 U.S.C. §102(b) as being anticipated by *Temma et al.*, U.S. Patent No. 5,796,996. Claims 8-9, 18, 20, and 22 were rejected under 35 U.S.C. §103(a) as being unpatentable over *Temma et al.*

The following remarks are provided in support of the pending claims and responsive to the Office Action of March 17, 2004 for the pending application.

I. Rejection of claims 1-2, 10-11, 16, 21, 23, and 25 under 35 U.S.C. §102(b)

In the Office Action of October 2, 2003, the Examiner assigned to the application rejected claims 1-2, 10-11, 16, 21, 23, and 25 under 35 U.S.C. §102(b) as being anticipated by *Temma et al.* ('996). The *Temma et al.* patent ('996) relates to a single CPU and a method by which that CPU executes a instruction. *Temma et al.* does not show two or more CPUs, as claimed by Applicant with the word "each". The dictionary definition of the word "each" is "every one of two or more" [1]. *Temma et al.* specifically relates to a single CPU performing an instruction, and does not teach or suggest application to multiple CPUs, as claimed by Applicant. Furthermore, *Temma et al.* does not show any "force" associated with the memory barrier execution. Rather, *Temma et al.* shows force associated with ejection of the output buffer. To clarify, the output buffer of *Temma et al.* is not equivalent to the memory barrier instruction of Applicant. See Col. 3, lines 20-21. In addition, upon completion of the instruction, the CPU of

[1] WEBSTER'S DICTIONARY 293 (encyclopedic ed. 1989), attached as Exhibit A.

Temma et al. receives an indicator. "[T]he completion of the ejection is notified to the CPU 700 together with a response of the real data by the execution of the read instruction." Col. 4, lines 2-5. The indicator of *Temma et al.* comes from a device or memory to the CPU, and does not originate from the CPU as claimed by Applicant. Finally, *Temma et al.* provide support to prevent interrupts, but does not provide support for sending an interprocessor interrupt. There is a clear distinction between these two elements. Accordingly, the execution of the instruction as well as the response associated with completion of the instruction of *Temma et al.* operate under different parameters and a different environment than that claimed by Applicant.

Applicant's invention *forces* each CPU, *i.e.* two or more CPUs, to execute a memory barrier instruction. The execution of the memory barrier instruction invalidates stale data and ensures that reading CPUs will access new data in a modified data structure. Upon completion of the memory barrier instruction, each CPU sends a communication to indicate completion of the memory barrier instruction. This step ensures a recordation in a common location indicating completion of the memory barrier instruction. Accordingly, the execution of a memory barrier instruction of Applicant clearly implies an action taken by two or more CPUs to enable a writing CPU to ensure invalidation of old data prior to updating a pointer to the data structure for new data.

There is no teaching in *Temma et al.* for forcing each CPU, *i.e.* two or more CPUs, to execute a memory barrier instruction. *Temma et al.* teaches force associated with an ejection of the output buffer, but this is not equivalent to forcing multiple CPUs to execute a memory barrier instruction. The force of *Temma et al.* is only associated with what may be considered a portion of a memory barrier instruction, but does not attach to a complete memory barrier instruction as claimed by Application.

In addition, there is no teaching in *Temma et al.* to send an interprocessor interrupt to all CPUs as a part of the step of forcing the CPUs to execute the memory barrier instruction. To be clear, in interprocessor interrupt indicates an interrupt between at least two processors. At a

minimum, one processor is sending the interrupt and another processor is receiving the interrupt. *Temma et al.* does not teach in interprocessor interrupt. Rather, *Temma et al.* teaches the single CPU set to an "interruption masking state", Col. 3, line 14, and an interruption program in response to an external interruption, Col. 4, lines 40-43. However, Applicant is claiming "an interprocessor interrupt to all CPUs". See claim 2. The interruption masking state is a state of operation of the CPU following receipt of an interrupt instruction. It is not equivalent to the actual interprocessor interrupt as claimed by Applicant. Furthermore, the interruption program of *Temma et al.* is a device interrupt, not an interprocessor interrupt. The external interrupt of *Temma et al.* originates from an external device, whereas an interprocessor interrupt has a local point of origination. Accordingly, it is clear that *Temma et al.* does not teach sending an interprocessor interrupt to multiple CPUs.

There is also no teaching in *Temma et al.* for a CPU to send an indicator to communicate completion of the memory barrier instruction. In fact, *Temma et al.* functions on the opposite principle. The CPU of *Temma et al.* is adapted to receive an indicator not to send an indicator.

In order for the claimed invention to be anticipated under 35 U.S.C. §102(b), the prior art must teach all claimed limitations presented by the claimed invention. "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." MPEP §2131 (citing *Verdegaal Bros. v. Union Oil Co. of California*, 814 F. 2d 628, 631, 2 U.S.P.Q. 2d 1051, 1053 (Fed. Cir. 1987)). As mentioned above, *Temma et al.* does not show all of the elements as claimed by Applicant in pending claims 1-2, 10-11, 16, 21, 23, and 25. Specifically, *Temma et al.* does not teach the use of force associated with execution of a memory barrier instruction by two or more CPUs, rather *Temma et al.* merely shows synchronous execution between a writing operation of the memory mapped register with execution of a CPU instruction. See Col. 3, lines 18-20. The only element of force present in *Temma et al.* is ejection of the output buffer. With respect to communication of the completion of the memory barrier instruction, the CPU of *Temma et al.* receives an indicator. See Col. 4, line 3. It does not send an indicator. However, the CPU of Applicant sends an

indicator in response to completion of the memory barrier instruction. The act of receiving and sending are two independent and different act. Accordingly, *Temma et al.* clearly fails to teach the limitations pertaining to the memory barrier instruction as presented in Applicant's pending claims 1-2, 10-11, 16, 21, 23, and 25.

Finally, "[a] previous patent anticipates a purported invention only where, except for insubstantial differences, it contains all of the same elements operating in the same fashion to perform an identical function." *Saunders v. Air-Flo Co.*, 646 F.2d 1201, 1203 (7th Cir. 1981) citing *Popeil Brothers, Inc. v. Schick Electric, Inc.*, 494 F. 2d 162, 164 (7th Cir. 1974) (holding patents were not invalid as being anticipated by or obvious in light of prior art). *Temma et al.* does not anticipate the invention of Applicant based upon the legal definition of anticipation. Although the prior art cited by the Examiner relates to a processor and instructions associated therewith, *Temma et al.* fails to show each and every element as presented in Applicant's claimed invention. In fact, *Temma et al.* does not show two or more CPUs being forced to execute a memory barrier instruction, each CPU sending an indicator in response to completion of the memory barrier instruction, or sending an interprocessor interrupt in association with force of the memory barrier instruction. Rather, *Temma et al.* shows a CPU execution of an instruction, followed by receipt of the CPU of notification of completion of ejection of the output buffer. Accordingly, Applicant respectfully requests that the Examiner remove the rejection of claims 1-2, 10-11, 16, 21, 23, and 25, and provide allowance of this application.

II. Rejection of claims 8-9, 18-20, and 22 under 35 U.S.C. §103(a)

In the Office Action dated March 17, 2004, the Examiner assigned to the application rejected claims 8, 9, 18-20, and 22 under 35 U.S.C. §103(a) as being unpatentable over *Temma et al.*, U.S. Patent No. 5,796,996.

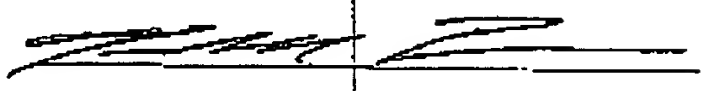
The discussion of *Temma et al.* above is hereby incorporated by reference.

Applicant's invention functions on a different principle than that taught in *Temma et al.* The *Temma et al.* patent does not force each CPU to execute a memory barrier instruction, nor require each CPU to send an indicator to communicate completion of the memory barrier instruction. The Examiner takes Official Notice regarding the use of an array for CPUs to register memory barrier requests, as well as the selection of mediums. Applicant hereby objects to the Official Notice taken by the Examiner. "The examiner must provide specific factual findings predicated on sound technical and scientific reasoning to support his or her conclusion of common knowledge." MPEP §2144.03(B). The Examiner has not provided the factual basis for the Official Notice. Furthermore, "[T]he mere fact that the prior art could be so modified would not have made the modification obvious unless the prior art suggested the desirability of the modification." *In re Gordon et al.*, 733 F.2d 900, 221 USPQ 1125, 1127 (Fed. Cir. 1984). *Temma et al.* does not suggest the use of an array to register memory barrier requests. Nor has the Examiner provided a teaching in the art that supports the use of an array to register a memory barrier request. It is axiomatic that the subject matter of the claims may not be considered obvious as a result of a hypothetical combination of references unless something in the references suggests that an advantage may be derived from combining their teachings. In this respect, the CAFC appears to speak directly to the issue of the need to determine the scope and contents of the prior art. Accordingly, the determination as to what may be within the scope and contents of the prior art serves to establish the parameters of what art may even be considered in determining the obviousness of an invention.

Furthermore, claims 8-9, 18-20, and 22 are dependent claims. Applicant contends that the elements taught in independent claims 1, 10, and 21 are not anticipated by *Temma et al.*, as discussed above. Since *Temma et al.* does not teach all of the elements present in the rejected independent claims, Applicant respectfully requests removal of the rejected dependent claims. Accordingly, removal of the rejection of claims 8-9, 18-20, and 22 under 35 U.S.C. §103(a) as being unpatentable over *Temma et al.* ('996) is respectfully requested.

For the reasons outlined above, withdrawal of the rejection of record and an allowance of this application are respectfully requested.

Respectfully submitted,

By: 

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